031611 Set - I

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Answers to Short / Objective Questions

SET - I

1. (i) (a) 3 (b) 4 (c) 2 (d) 1

(ii) (a) It Controls the entire operations of the microprocessor.

(b) It Controls all peripherals connected to microprocessor.

(c) It generates timing and control signals required for the execution of the instruction.

(d) It Controls data flow between CPU and peripherals/Memory.

(iii) (a) 1-byte instruction (b) 2-byte instruction

(c) 3-byte instruction

(iv) In SUB M the Content of memory location addressed by HL pair is Subtracted from the Content of the accumulator. The result is placed in the accumulator. But in CMP M instruction, although the Content of the memory location addressed by HL pair is Subtracted from the Content of accumulator, the content of the accumulator remains unchanged. Result is discarded.

(v) In EEPROM need not to be removed from the System board for erasing the Contents but

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EPROM is to be removed from the System for erasing. EEPROM is byte erasable. But in EPROM all Contents will be erased when it will be exposed to high intensity short wave ultra-violet light.

(vi) A Dynamic RAM loses its stored information in a few milliseconds even though its power supply is on. When a Dynamic RAM and Control and ~~refet~~ refresh circuit is fabricated on a single chip it is known as i-RAM.

(vii) Software - Software is a set of programs
Hardware - The physical devices and electronic circuitry of a Computer are Called Hardware.
Firmware - The programs stored in ROMs, PROMs, EPROMs, EEPROMs or in flash memory are known as firmware.

(viii) In Asynchronous data transfer Scheme, microprocessor initiates an I/O device to get ready. Microprocessor goes on checking ~~Continuously~~ continuously the status of I/O device whether it is ready or not. During this period, it is not executing main program. But in interrupt driven data transfer Scheme, after initiating an I/o device to get ready, it executes its main program instead of remaining in a program loop to check the status of the I/o device.

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(ix) In PUSH B instruction the contents of Register pair BC is pushed into the stack where as in PUSH PSW the content of accumulator and the word formed with the contents of status flags are pushed into the stack.

(X) Addressing Modes of INTEL 8086 :-

(a) Register Addressing - MOV AX, CX

(b) Immediate Addressing - MOV AL, 35H

(c) Direct Addressing - ADD AL, [0301]

(d) Register Indirect Addressing - MOV AX, [BX]

(e) Based Addressing - MOV AL, [BX+05]
05 is 8 bit displacement.

(f) Indexed Addressing - MOV AX, [SI+05]

(g) Based Indexed Addressing - ADD AX, [BX+SI]

(h) Based Indexed with Displacement -
MOV AX, [BX+SI+05]

RK

Answers to Short Objective Questions

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latch or in memory. when ALE signal will be made high during T_1. $\overline{WR}$ goes low in T_2 indicating that the write operation is to be performed. In T_3 $\overline{WR}$ goes high and the write operation is terminated.

In I/O Write Cycle the CPU sends data to an I/O port or I/o device from the accumulator. It is similar to Memory Write Cycle. In Case of I/O Write Cycle, IO/$\overline{M}$ goes high indicating that the address sent out by the CPU is for I/O device or I/O port. Signal; S_1, S_0, ALE, and $\overline{WR}$ Signal will be same as shown in figure for Memory Write Cycle. In Case of I/o device or I/O port the address is only 8 bits and therefore the address of I/o device is duplicated on both ~~A and AD~~ Address and Address-data bus.

2.(b) pending Interrupt – When one interrupt request is being served, other interrupt may occur resulting in a pending request. When more than one interrupts occurs simultaneously, the interrupt having higher priority is served and the interrupts with lower priority remain pending.

SIM – It is known as Set Interrupt Mask. The execution of this instruction enables/disables Maskable interrupts

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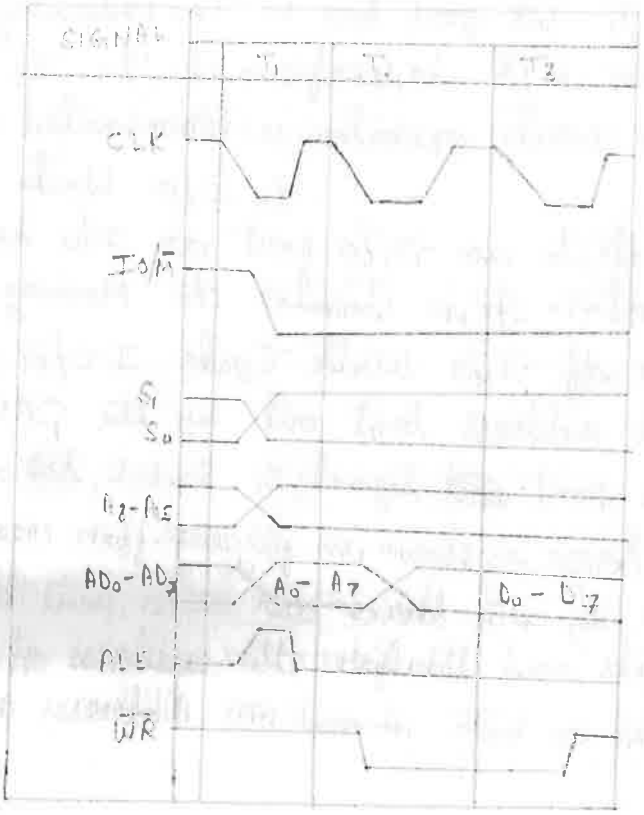
Sets (I) / (II)

2. (a) Timing diagram of Memory Write Cycle.



1st Signal IO/M will be low because in write operation CPU sends data from the accumulator or any other register to memory. In 2nd Signal, So will be 1 and S_1 will be 0 for Write operation. In 3rd Signal ~~that is~~ $A_8 - A_{15}$, 8 MSBs of address will be transmitted through address line. 8 LSBs of address will be transmitted through data lines in 1st Clock Cycle T_1 as shown in figure. In Clock Cycle T_2 and T_3 data will be transmitted through data lines 8 LSBs transmitted through data line in 1st Clock Cycle will be latched in some external

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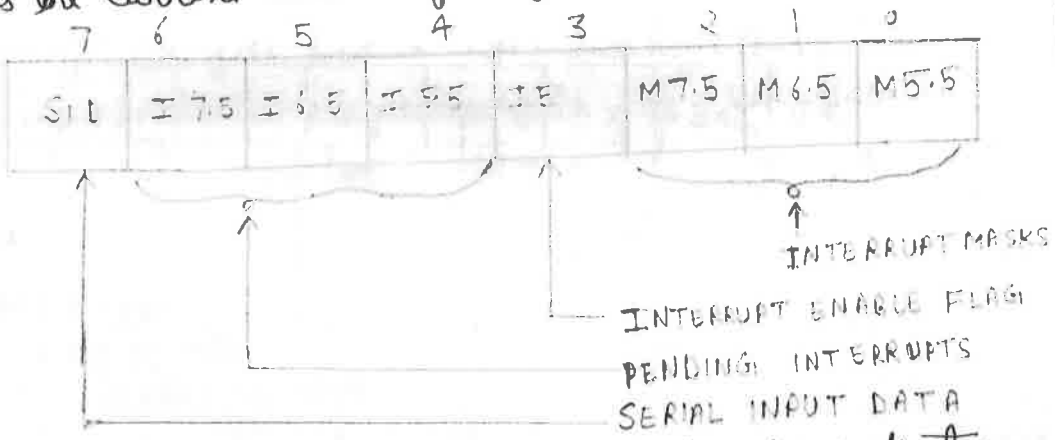
Sets (I) / (II)

It gives the current status of only maskable interrupts.



Bits 0-2 are for interrupt masks; 1 = masked. Bit 3 indicates interrupt enable flag; 1 = enabled. Bit 4-6 indicate pending interrupts; 1 = pending. Bit 7 - Serial input data, if any. After executing the interrupt service subroutine the processor checks whether any other interrupt is pending using RIM instructions. If an interrupt is pending the processor executes its interrupt service subroutine before it returns to the main program.

3. (a) figure given below shows the various registers of INTEL 8085

INTEL 8085 has the following registers :-

(i) One 8-bit accumulator i.e. register A
(ii) Six 8-bit general purpose registers - B, C, D, E, H and L
(iii) One 16-bit stack pointer, SP
(iv) One 16-bit program Counter, PC
(v) Instruction register
(vi) Temporary register

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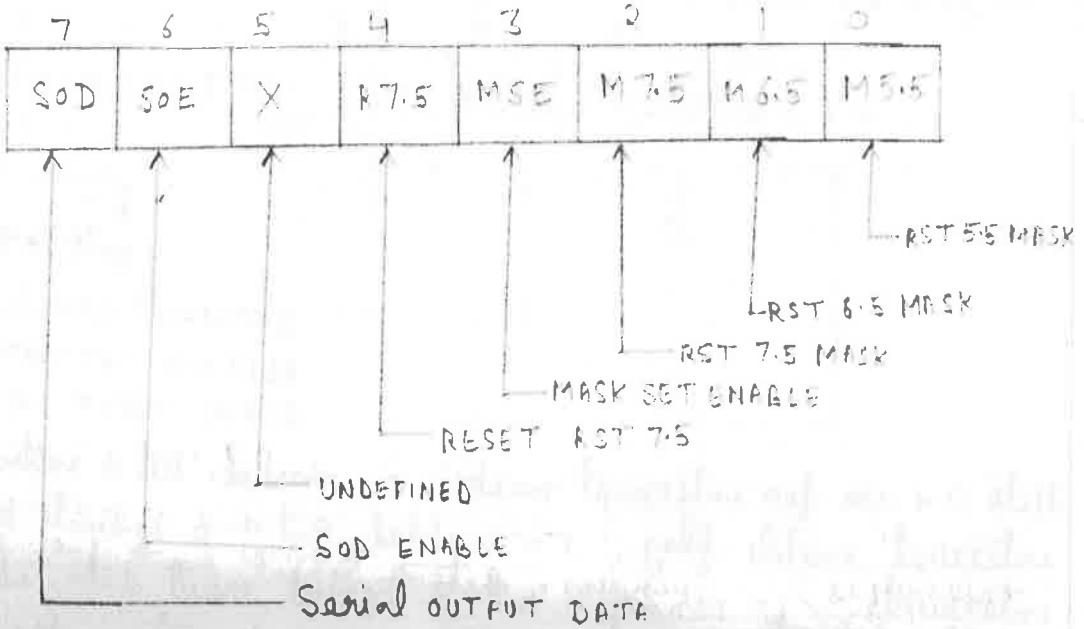
Sets (I) / (II)

according to the bit pattern of the accumulator.



Bit 0 is for RST 5.5 mask, bit 1 for RST 6.5 mask and bit 2 for RST 7.5 mask. If a bit is set to 1 the corresponding interrupt is masked off (disabled). If it is set to 0, the corresponding interrupt is enabled. Bit 3 is set to 1 to make bits 0-2 effective. Bit 4 is an additional control for RST 7.5. If it is set to 1, the flip flop for RST 7.5 is reset. Thus RST 7.5 is disabled regardless of whether bit 2 for RST 7.5 is 0 or 1. Bit 6 and 7 are for serial data output. Bit 6 is to enable SOD which will be 0. The content of bit 7 may be either high (1) or low (0)

RIM - It is known as Read Interrupt Mask which is used by programmer to know the current status of the pending interrupts.

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Sets (I) / (II)

Accumulator:- It is a 8 bit register known as accumulator. It is used to hold one of the operands of an arithmetic and logical operation. The final result of an arithmetic and logical operation is placed in the accumulator.

General purpose Registers:- INTEL 8085 Contains six 8 bit general purpose Registers. They are B, C, D, E, H and L. To hold 16 bit data, a register pair can be used. Valid register pairs are B-C, D-E and H-L.

Program Counter :- It is a 16 bit register used to hold the memory address of the next instructions to be executed.

Stack Pointer :- It is a 16 bit register which holds the address of the top element of the data stored in the stack.

Instruction Register :- It holds the opcode of the instruction which is being decoded and executed.

Temporary Register :- It is an 8 bit register associated with the ALU. It holds data during an arithmetic / logical operation. It is used by the microprocessor. It is not accessible to programmer.

In addition to the above mentioned registers, the 8085 microprocessor contains a set of five flip-flops which serve as flags (or status flags). A flag (or status flag) is a flip-flop which indicates some condition which arises after the execution of an arithmetic and logical instruction.

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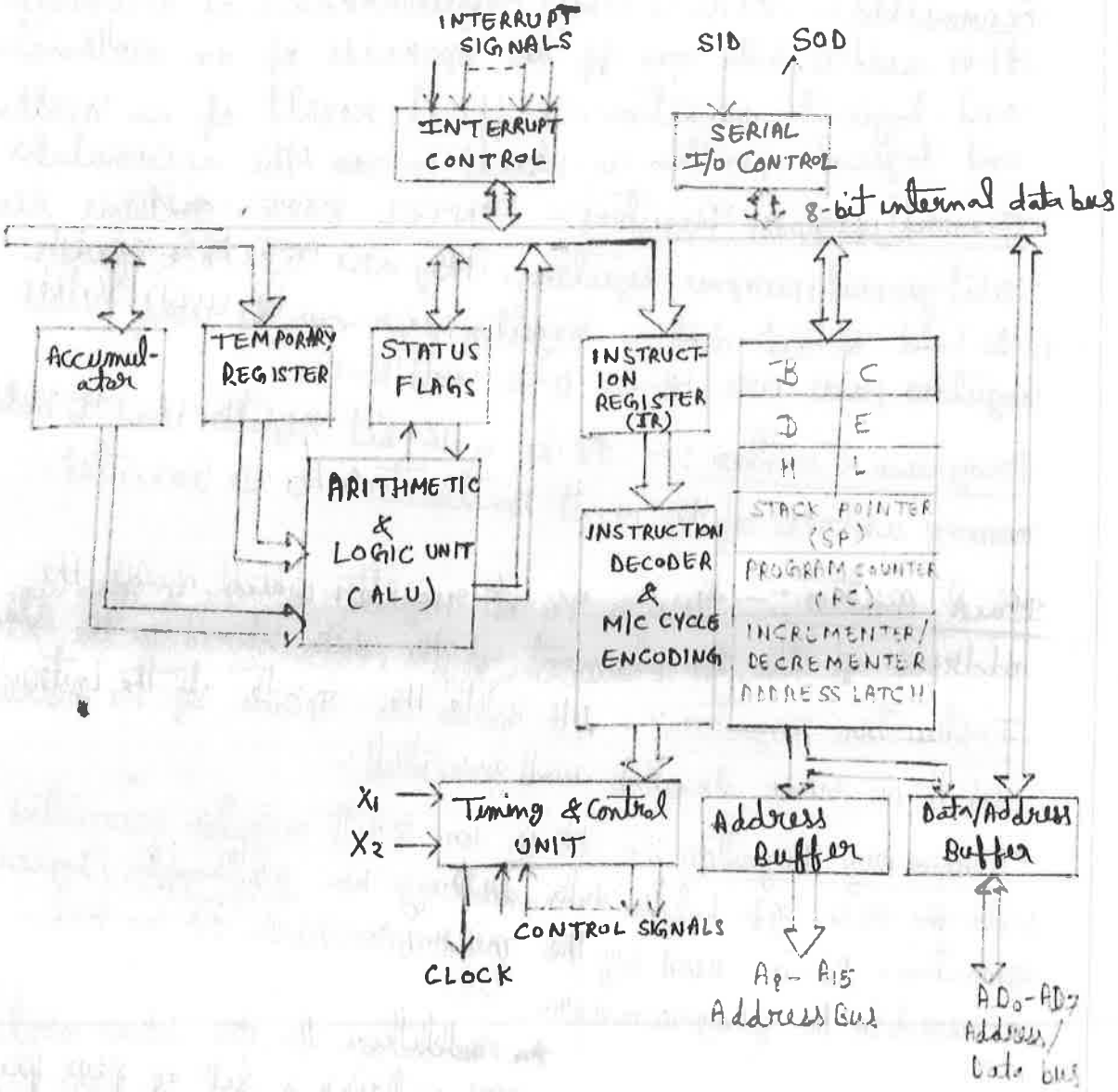
Sets (I) / (II)



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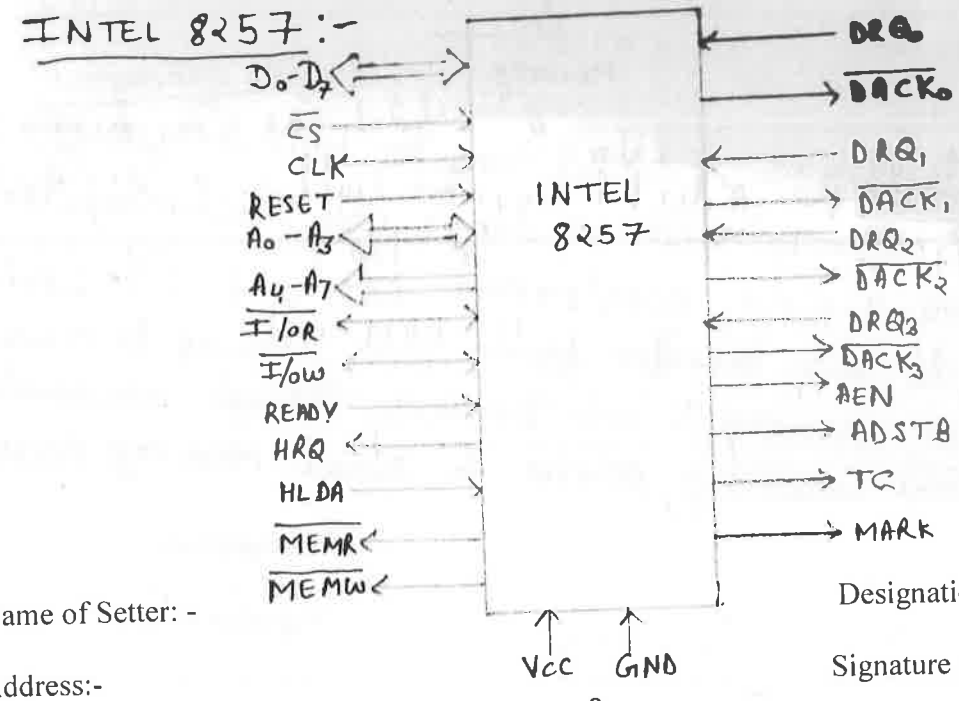
Sets (I) / (II)

technique is ~~proffered~~ preferred in Bulk data transfer. In DMA data transfer scheme, data is transferred directly between memory and I/O Devices. CPU doesnot participate. The data transfer is controlled by the I/o Device or a DMA Controller. For DMA data transfer, the I/o Device must have its own byte count register and memory address register ~~et~~. It must also be able to generate control signals required for DMA data transfer. Generally, I/o Devices having above features are not available in the market. Single chip programmable DMA controllers have been developed by several manufacturers for interfacing I/o Devices to the microprocessor for DMA data transfer.

INTEL 8257 :-



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arithmetical Sets (I) / (II)

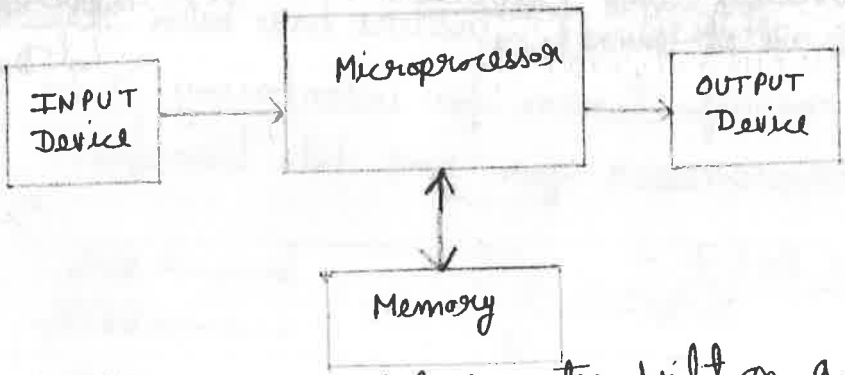
ALU :- All ~~arithmetical~~ and logical operations are performed by these unit.

Timing and Control unit :- It controls :-

(i) (a) The entire operations of the microprocessor.
(ii) (b) All peripherals connected to microprocessor.
(iii) (c) data flow between CPU and peripherals / Memory.
It also generates timing and control signals required for the execution of the instruction.

3.(b) Microprocessor :- The Central processing unit built on a single IC is known as Microprocessor.

Microcomputer :- A digital Computer in which one microprocessor has been provided to act as a CPU, is called Microcomputer.



Microcontroller :- A digital Computer built on a single IC is called Microcontroller or single chip Microcomputer. It Contains a CPU, ROM/EPROM, RAM and I/O Devices

4. (a) Bulk data transfer from I/O Devices to memory or from memory to I/O Devices through accumulator is a time Consuming process. So, Direct Memory Access

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Address:- Signature of Setter

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Sets (I) / (II)

$A_0 - A_7$:- These are address lines.

$D_0 - D_7$:- These are data line. During DMA Cycle, the 8257 sends the 8 MSBs of the memory address through these lines at the beginning of the DMA Cycle. These 8 MSB s are then latched in 8212 latch. Thereafter the data bus is made available to handle memory data transfer during rest of the DMA Cycle.

AEN :- Address latch enable

ADSTB :- A HIGH on this line latches the 8 MSBs of the address, which are sent on D- bus, into intel 8212 connected for this purpose.

$\overline{CS}$:- It is chip select.

$\overline{IOR}$:- It is bidirectional I/o read line.

$\overline{IOW}$:- It is bidirectional I/O write line.

$\overline{MEMR}$:- Memory read

$\overline{MEMW}$: Memory write

TC :- Byte Count

MARK :- Modulo 128 Mark

CLK :- Clock

HRQ :- Hold request

HLDA :- Hold acknowledge.

An I/o device sends its request for DMA transfer through one of the four DRQ lines. On receiving the DMA request for DMA data transfer from an I/o device, the intel 8257

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Sets (I) / (II)

It is a 40 pin IC package and requires +5V DC supply for its operation. Four I/O Devices can be interfaced to the microprocessor through this device. It is a 4-channel programmable DMA Controller. Each channel incorporates two 16-bit registers – (1) DMA address register (2) byte Count register. These registers are initialised before a channel is enabled. Initially the DMA address register is loaded with the address of the first memory location to be accessed. During DMA operation it stores the next memory location to be accessed in the next DMA Cycles. 14-LSBs of the byte Count register store the number of bytes to be transferred. 2^{14} (16384) bytes of data can directly be transferred to the memory from the I/O device or from the memory to the I/O device. 2 MSBs of the byte Count register indicate the operation which will be performed by the Controller on that channel.

Important pins :-

$\overline{DRQ_0} - \overline{DRQ_3}$:- These are request line. An I/O device sends its DMA request on one of these lines.

~~DACK0 – DACK3~~

$\overline{DACK_0} - \overline{DACK_3}$:- These are DMA acknowledge lines. The Intel 8257 sends an acknowledge signal through one of these lines informing an I/O device that it has been selected for DMA data transfer.

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Sets (I) / ~~(II)~~

I/o device whose address is in H-L pair.

I/o Mapped I/o Scheme :-

In this scheme, the addresses assigned to memory locations can also be assigned to I/o devices. Since the same address may be assigned to a memory location or an I/o device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/o device. The intel 8085 issues an $IO/\overline{M}$ signal for this purpose. When this signal is high the address on the address bus is for an I/o device. When this signal is low, the address on the address bus is for a memory location. Two extra instructions IN and OUT are used to address I/o devices. The IN instruction is used to read the data of an input device. The OUT instruction is used to send data to an output device. This scheme is suitable for a large system.

~~5~~ ~~(a)~~

Name of Setter: -

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Address:-

Signature of Setter

Sends the hold request to the CPU through the HRQ line. The 8257 receives the hold acknowledge signal from the CPU through HLDA line. After receiving the hold acknowledge from the CPU, it sends DMA acknowledge to the I/O device through $\overline{DACK}$ line. Then data will be transferred between I/O device and memory. The byte Count is decremented by one after the transfer of one byte of data. When byte Count becomes zero, TC goes high indicating that the data transfer using DMA is Complete.

4. (b) Memory Mapped I/O Scheme :- In memory mapped I/O scheme there is only one address space. Some addresses are assigned to memories and some addresses to I/O devices. An I/O device is also treated as a memory location and one address is assigned to it. The addresses for I/O devices are different from the addresses which have been assigned to memories. Each and every memory location and I/O devices will be assigned one unique address. The addresses which have not been assigned to memories can be assigned to I/O devices.

In this scheme all the data transfer instructions of the microprocessor can be used for both memory as well as I/O devices. For example, MOV A, M will be valid for data transfer from the memory location or

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Sets (I) / ~~(II)~~

2011	32, 50, 24		STA	2450 H	Smallest number stored in accumulator will be transferred to memory location 2450 H
2014	76		HLT		The ~~prior~~ execution will be STOPPED

Example ~~1~~ –

DATA
2500 – 03H (Count)
2501 – 86H
2502 – 58H
2503 – 75H

Result –
2450 – 58H

5. (b) (i) READY :- It is a signal sent by an I/O Device to microprocessor which indicates that I/O device is ready to send or receive data. A slow I/O device is connected to the microprocessor through READY line. ~~The~~ When Microprocessor wants to send/receive data from I/O device, microprocessor will check the status of READY signal. When a READY is low microprocessor waits till READY becomes high. When READY is high, it indicates that I/O device is ready to send or receive data

(ii) RESET IN :- It resets the program counter to zero. It also resets interrupt enable and HLDA flip flops.

(iii) INTA :- It is an interrupt acknowledge signal issued by the microprocessor after receiving ~~an~~ an interrupt request ~~from~~ from an external device. It is a low active signal.

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Sets (I) / (II)

5. (a)

Address	Machine Codes	Labels	Mnemonics	Operands	Comments
2000	21,00,25		LXI	H, 2500H	2500 will be stored in HL pair.
2003	4E		MOV	C, M	Count will be stored in register C
2004	23		INX	H	Memory address of 1st number will be stored in HL pair.
2005	7E		MOV	A, M	1st number will be stored in accumulator.
2006	0D		DCR	C	Count will be decremented by one.
2007	23	LOOP	INX	H	Memory address of memory location in which 2nd number is stored will be transferred to HL pair.
2008	BE		CMP	M	2nd number will be compared with 1st number.
2009	DA,0D,20		JC	AHEAD	If there is Carry program will go to AHEAD
200C	7E		MOV	A, M	If there is no Carry, 2nd number will be transferred to accumulator.
200D	0D	AHEAD	DCR	C	Count will be decremented by one.
200E	C2,07,20		JNZ	LOOP	If Count number does not come to zero, program will go to LOOP and if Count number comes to 0 program will go downward.

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Sets (I) / (II)

the desired input signal. When microprocessor wants to switch on a particular channel of the multiplexer, appropriate logic will be sent to Multiplexer through PC_0, PC_1, PC_2. A/D Converter is a slow device, so it will take some time to Convert analog voltage into digital form. During this period, the analog voltage should be kept constant. For this purpose, a Sample and Hold circuit is used in case of ~~DC~~ AC input. The S/H ckt samples the instantaneous Value of AC signal at the desired moment and holds it constant during the Conversion period. It will get ~~logic~~ pulse through PB_1 as shown in figure.

When a particular channel is to be used, microprocessor will send appropriate logic to multiplexer through PC_0, PC_1, PC_2. Signal will go to ADC through S/H ckt. Microprocessor will send start of conversion signal (S/C) to ADC through PC_3. ADC is a slow device. It will take some time to convert analog signal to digital form. When conversion is over, it will send end of conversion signal (E/C) to I/o port through PC_7. Then Microprocessor will send command to output data at port A.

6. (b) Operating modes of 8255 :-

(i) Mode 0 - In Mode 0 operation, each of four ports can be programmed to act as an input or output port.

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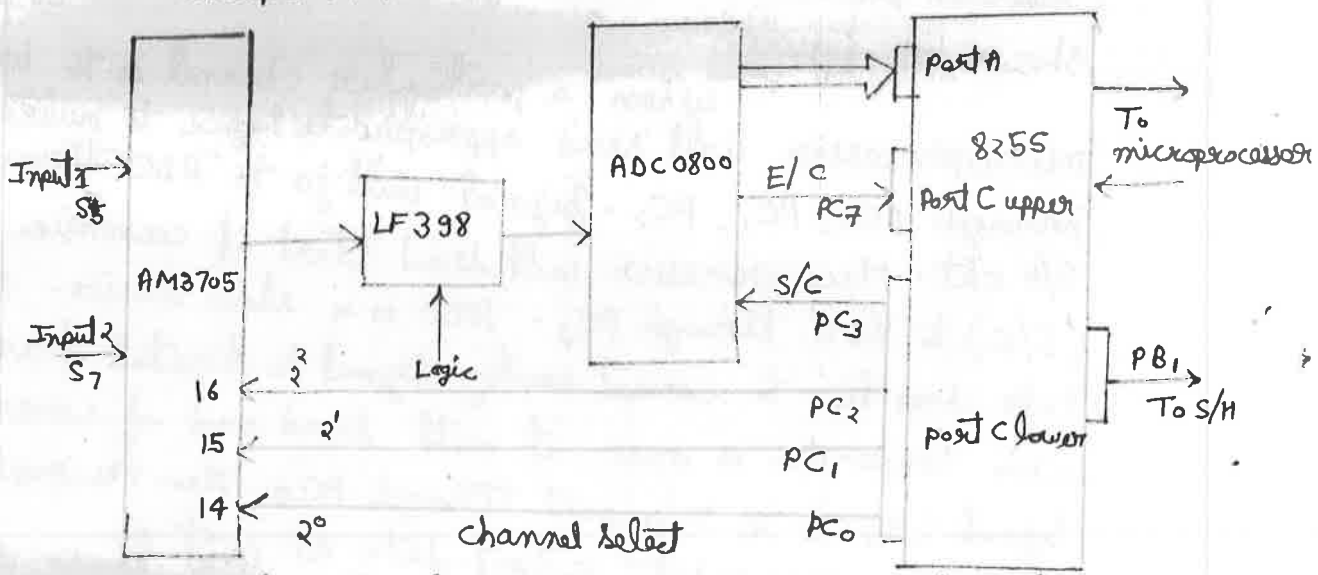
Sets (I) / (II)

(iv) SID :- It is data line for serial input. The data on this line is loaded into the 7th bit of the accumulator when RIM instruction is executed.

(v) HOLD :- When another device of the computer system, requires address and data buses for data transfer, it sends HOLD signal to the microprocessor.

(vi) X_1, X_2 :- These are terminals to be connected to an external Crystal oscillator which drives an internal circuitry of the microprocessor to produce a suitable clock for the operation of microprocessor.

6. (a) Interfacing of ADC 0800, Analog Multiplexer and Sample and Hold



When analog inputs are more than one, and analog multiplexer is connected in the interfacing circuit. Microprocessor sends appropriate command to the multiplexer to switch ON the desired channel to obtain

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Sets (I) / (II)

5V dc. In a multiprocessor system it operates in the maximum mode. In case of Maximum mode of operation Control signals are issued by INTEL 8288 bus Controller. When this signal is made low, CPU operates in Maximum Mode, and it is grounded.

(iii) HOLD :- When another device in microcomputer system wants to use buses, it sends a HOLD request to CPU through this pin. It is used in Minimum Mode of operation.

(iv) $\overline{TEST}$:- When it is low the microprocessor continues execution otherwise waits.

(V) $\overline{RQ}/\overline{GT_1}$, $\overline{RQ}/\overline{GT_0}$:- It is bidirectional local bus priority control used in Maximum Mode of operation. Other processors ask the CPU through these lines to release the local bus. $\overline{RQ}/\overline{GT_0}$ has higher priority than $\overline{RQ}/\overline{GT_1}$

(vi) $AD_0 - AD_{15}$:- It is bidirectional Address/data lines. These are low order address bus. They are multiplexed with data. 8 LSBs of data are transmitted on $AD_0 - AD_7$ and 8 MSBs of data on $AD_8 - AD_{15}$

(b) (i) MOV AX, [BX + DISP] :- The Content of Memory address stored in BX will be added with displacement. The Content of this new memory location will be transferred to AL and the Content of next memory location will be transferred to AH.

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Sets (I) / (II)

(ii) Mode 1 - It is ~~stroked input~~ strobed input/output mode of operation. Port A and port B both are designed to operate in this mode of operation. PC_0, PC_1 and PC_2 are used for the control of the port B which can be used either as input or output port. If the port A is operated as an input port, PC_3, PC_4 and PC_5 are used for its control. The remaining pins of port C i.e. PC_6 and PC_7 can be used either input or output. When port A is operated as an output port, pins PC_3, PC_6 and PC_7 are used for its control. The pins PC_4 and PC_5 can be used either as input or output.

(iii) Mode 2 - It is strobed bidirectional Mode of operation. In this mode only port A can be programmed to operate. ... used to control port A.

7. (a) (i) LOCK :- It is an active low signal. When it is low all interrupts are masked and no HOLD request is granted. In multiprocessor system all other processors are informed by this signal that they should not ask the CPU for giving up control over buses.

(ii) MN/$\overline{MX}$:- There are two modes of operation for INTEL 8086, Namely the Minimum Mode and Maximum Mode. When only one 8086 CPU is to be used in a microcomputer system, the 8086 is used in the minimum Mode of operation. In this Mode the CPU issues the control signals required by memory and I/O devices. For Minimum Mode of operation the pin MN/$\overline{MX}$ is connected to 5V dc.

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Sets (I) / ~~(II)~~

remainder will be placed in AH. When dividend in 32-bit and divisor is 16 bit then 16 bit quotient will be placed in AX and the 16 bit remainder will be placed in DX.

(vi) MOV [BX], 1439H :- 1439 data will be transferred to two consecutive memory locations. ~~1st one~~ Memory address of 1st memory location ~~will be~~ is stored in BX.

8. (a) Delay Subroutine using two registers :-

Memory address	Machine Codes	Labels	Mnemonics	Operands	Comments
2400	06, 10		MVI	B, 10H	desired number 16(decimal) will be stored in register B
2402	0E, 78	LOOP I	MVI	C, 78H	2nd number 120(decimal) will be stored in register C
2405	0D	LOOP II	DCR	C	Content of register C will be decremented by one.
2406	C2, 05, 24		JNZ	LOOP II	If Content of register C doesn't come to zero program will go in LOOP II but if Content of C is zero, program will go downward.
2409	05		DCR	B	Content of register B will be decremented by One.
240A	C2, 02, 24		JNZ	LOOP I	If Content of register B doesn't come to 0, the program will go to LOOP I otherwise program will go downward ~~there~~ program will go to main
240D	C9		RET		

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Sets (I) / (II)

(ii) MOV [0301], CX :- Contents of CX will move to 0301 and 0302.

(iii) ADD [BX], CX :- ~~Content of CX and content of Memory location BX which is memory address an~~ Content of Memory location whose address is stored in BX and content of next memory location will be added to the content of CX.

(iv) IMUL CX :- ~~This~~ instruction is used for multiplication ~~of signed numbers. One of the number, I~~ of two 16 bit signed numbers. One of the operand is placed in AX and the other is in CX. So, Content of AX and content of CX will be multiplied and the result will be placed in AX and DX.

(V) DIV [BX] :- This instruction is used for deviding a 32-bit or 16-bit number by a 16 bit or 8-bit number. It is used for unsigned numbers. If the dividend is 32-bit, it will be placed in DX and AX and the 16-bit divisor will be placed in two consecutive memory locations. 1st memory location will be stored in BX. But if the dividend is of 16 bit it will be placed in AX and 8-bit divisor will be placed in a memory location. That memory address will be stored in BX. The 8 bit quotient will be placed in AL, and the 8-bit

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Sets (I) / ~~(II)~~

(ii) XRA B

B - 01001001
A - 00111010
XRA B - 01110011

Flags:-
CS = 0
AC = 0
Z = 0
P = 0
S = 0

program
MVI A, 3AH
MVI B, 49H
XRA B
STA 8520H
HLT

(iii) ORA B

A - 00111010
B - 01001001
ORA B - 01111011

Flags:-
CS = 0, AC = 0, Z = 0, P = 1, S = 0

program
MVI A, 3AH
MVI B, 49H
ORA B
STA 8520H
HLT

~~9. (a)~~

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Sets (I) / ~~(II)~~

~~Ende~~

Instructions	STATES	How many times the instruction states is executed.	
MVI B, 10H	7	1	7X1
~~LOOP:~~ MVI C, 78H	7	16	7X16
DCR C	4	120X16	4X120X16
JNZ	7/10	120X16	10X(120-1)X16+7X16
DCR B	4	16	4X16
JNZ	7/10	16	10X(16-1)+7X1
RET	10	1	1X10

Total states = 27182

Delay time = $27182 \times 320 \times 10^{-9}$ second = 8.6912 ms.

(b) A → 3A
B → 49
(1) SUB B

49 = 01001001
1's Complement of 49 H = 10110110
2's Complement of 49 H = 10110110 + 1 = 10110111

Now A − B = A + (2's complement of 49)
= 00111010 + 10110111
= 11110001

Flags.

Z = 0
P = 0
AC = 1
C = 0

Program

~~MVI A, 3H~~
~~MOV B, 49H~~
MVI A, 9H
CMA
INR A
MOV B, A
MVI A, 3A
ADD B
STA 8520H
HLT

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Sets (I) / (II)

The directional flag (DF) is used in string operation. If it is set to 1, string bytes are accessed from higher memory addresses to lower memory address. When it is set to zero, the string bytes are accessed from lower memory addresses to higher memory addresses. Other flags are same as those available in INTEL 8085.

(b) Execution unit :- The general purpose registers, stack pointer, base pointer and index registers, ALU, Flags, Instruction Decoder and Timing and Control unit constitute execution unit. The Execution unit receives Opcode of an instruction from the Queue, decodes it and then executes it.

Bus interface unit :- The segment registers, instruction pointer and 6-byte instruction Queue are associated with the bus interface unit. BIU handles transfer of data and addresses between the processor and memory/I/o devices. It computes and sends out addresses, fetches instruction codes, stores fetched instructions code in a First-IN-First-OUT Register set Called a Queue, reads data from memory and I/o devices, writes data to memory and I/o devices.

pipelining :- The Bus interface unit and Execution unit operate in parallel independently. While EU executes

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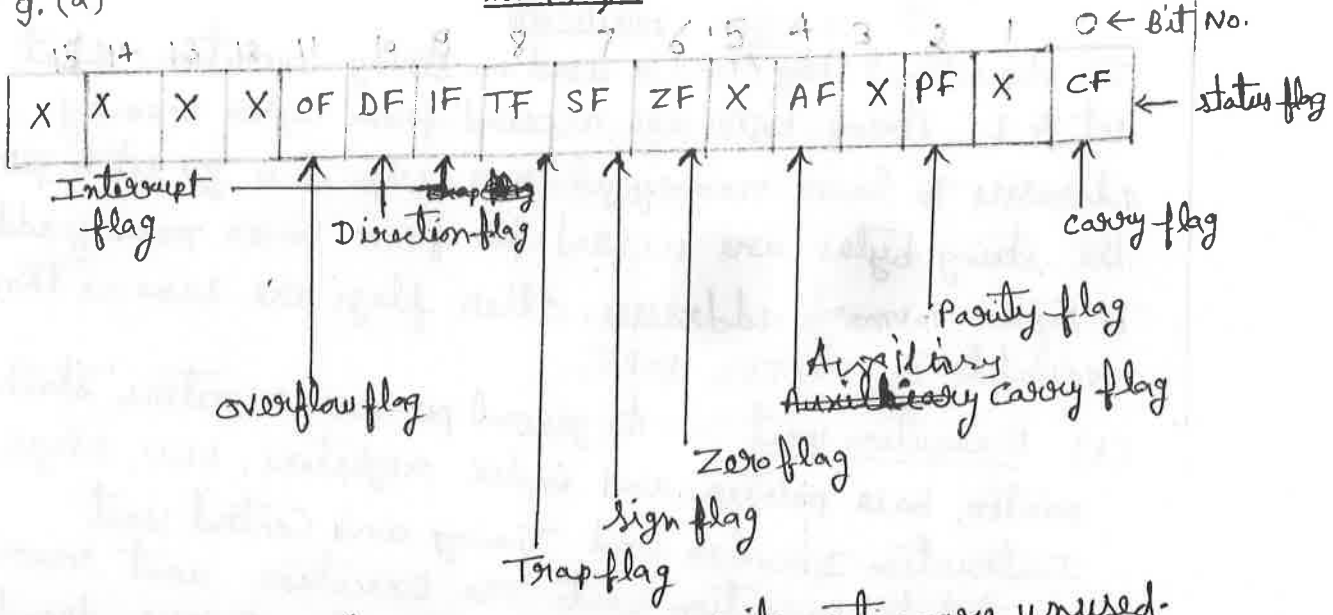
g. (a) Sets (I) / ~~(II)~~



There are 9 states flags and seven bit positions are unused. Out of 9 flags 6 are Condition flags and 3 are Control flags. 6 Condition flags are Carry, Auxiliary Carry, Zero, Sign, parity and overflow flags. These flags are set/Reset by the processor after the execution of an arithmetic and logical instructions. Three control flags are trap, interrupt and directional. These flags are Set/Reset by the programmer as required by certain instructions in the program. The overflow flag is set to 1, if the result of a signed operation becomes out of range, otherwise it is reset i.e. it is made 0. When the trap flag (TF) is set to 1, a program can be run in single-step mode. The interrupt flag (IF) is set to 1 to enable INTR of 8086. If it is 0, INTR is disabled.

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Sets (I) / ~~(II)~~

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Sets (I) / (II)

instructions, the BIU fetches instructions. This type of overlapped operation of the functional units of a Microprocessor is called pipelining.

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