Paper Code : 05/602

B.TECH. 6TH SEMESTER EXANIMATION, 2014

Answers to Short / Objective Questions

Answer 1.

i. (a) ii. (a) iii. (a) iv (e) v. (a) vi. (d)
vii.(b) viii.(c) ix. (c) x(d)

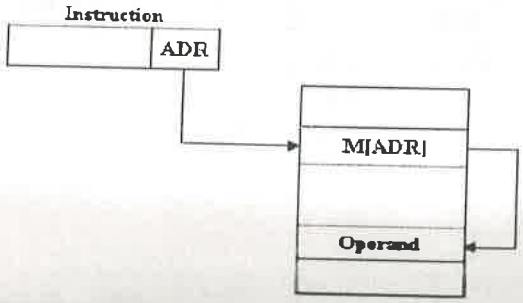
B.TECH. 6TH SEMESTER EXANIMATION, 2014

Answers to Short / Objective Questions

B.Tech 6th Semester Examination, 2014
Model Answer

Subject:- **Paper Code:-** 05/602

Sets (I) / (II)



Answer 3b)

(i) direct: 400
(ii) immediate: 301
(iii) relative: 302+400=702
(iv) register indirect: 200
(v) index with R1 as the index register: 200+400 = 600

Answer 4a)

	PC	SP	Top of Stack
Initial	1120	3560	5320
After Call	6720	3559	1122
After Return	1122	3560	5320

Answer 4b)

Branch Instruction- Branch without being able to return
Subroutine call: Branch to subroutine and then return to calling program
Program interrupt: Hardware initiated branch with possibility to return

Answer 4c)

External Interrupt: from I/O devices, from timing devices, from a circuit monitoring the power supply, any external sources etc.
Internal Interrupt: illegal or erroneous use of instruction or data, Register overflow, attempt to divide by zero, invalid opcode, stack overflow, protection violation etc
Software interrupt is a special call instruction that behaves like an internal interrupt rather than subroutine call.

Name of Setter: - Designation:-

Address:- Signature of Setter

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Model Answer

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Sets (I) / (II)

1	T1	T2	T3	T4	T5	T6	T7	T8					
2		T1	T2	T3	T4	T5	T6	T7	T8				
3			T1	T2	T3	T4	T5	T6	T7	T8			
4				T1	T2	T3	T4	T5	T6	T7	T8		
5					T1	T2	T3	T4	T5	T6	T7	T8	
6						T1	T2	T3	T4	T5	T6	T7	T8

$(K+N-1)\ T_p = 6+8-1 = 13$ cycles

Answer 9

Ans:

Associative Mapping

In case of associative mapping, the contents of cache memory are not associated with any address. Data stored in the cache memory are not accessed by specifying any address. Instead, data or part of data is searched by matching with the contents. In associative mapping method, both the word and the address of the word (in the main memory) are stored in the cache as shown in Figure. The address bits, sent by the CPU to search, are matched with addresses stored in the cache memory. If any address is matched, the corresponding word is fetched from the cache and sent to the CPU.

If not match is found in cache memory, the word is searched in the main memory. The word along with address is then copied from main memory into cache. If the cache is full, then the existing word along with its address must be removed to make room for the new word.

Associative mapping has the advantage that it is a very fast access method, but it has the disadvantage that it is very expensive and complicated because of complex logical circuits that ate required to implement data searching by content and not by address.

Due to the high cost associated with logic circuits required to implement associative mapping, other methods are used in which data is cache memory are accessed by address, like direct mapping and set associative mapping.

Name of Setter: -

Designation:-

Address:-

Signature of Setter

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Model Answer

Subject:- Computer Architecture

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Sets (I) / (II)

Answer 2. a)

The two register transfer statements are
P : R1 ← R2
P`Q: R1 ← R3

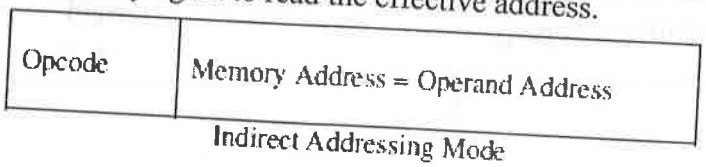
Answer 2b)

A subroutine is a self-contained sequence of instructions that performs a given computational task. During the program execution, a subroutine can be called many times to perform its operations. Each time a subroutine is called, a branch is executed to start executing its set of instruction and a branch is made back to the main program when the subroutine has been executed. The instruction that causes the transfer of program control to a subroutine is known by different names. Some common names are called subroutine, jump to subroutine or branch and save address.

The call subroutine instruction consists of an operation code and the address that specifies the beginning of subroutine. The instruction is executed by performing two operations (i) the address of the next instruction i.e. the return address in the program counter is stored at some temporary location, (ii) the control is transferred at the beginning of the subroutine. The last instruction of every subroutine, called as return from subroutine, transfers the return address stored in temporary location into the program counter. This return address helps in a transfer of program control to the instruction whose address was stored in temporary location. This temporary location can be the first memory location of the subroutine, or some fixed memory location or a processor register or can be a memory stack. But most efficient way is to store the return address in a memory stack.

Answer 3a)

In indirect addressing mode the address field of the instruction gives the address where the operand is stored in the memory. Control fetches the instruction from memory and uses its address part to access memory again to read the effective address.



Indirect Addressing Mode

For Example,
Effective address = M[ADR]
LD@ADR
AC ← M[M[ADR]]

Name of Setter: -

Designation:-

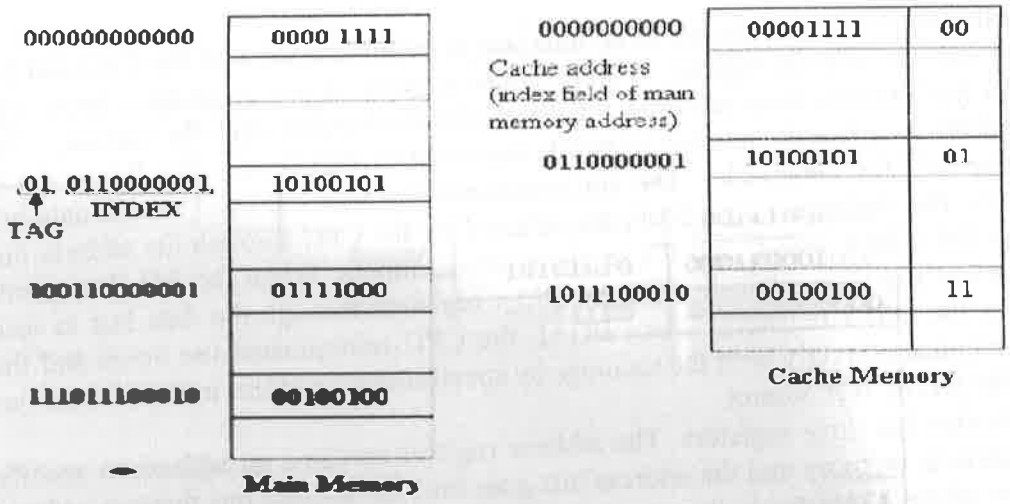
Address:-

Signature of Setter

B.Tech 6th Semester Examination, 2014
Model Answer

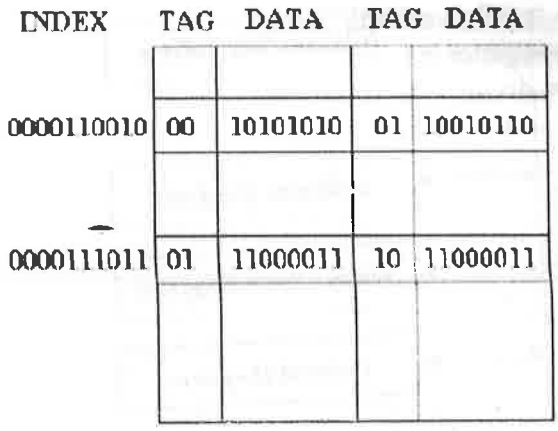
Subject:- Paper Code:-

Sets (I) / (II)



Set Associative mapping

The disadvantage of direct mapping is that two words with same index but different tag cannot be stored into cache at the same time. As an improvement to this disadvantage of direct mapping, a third type of cache organization called set associative mapping is used. In this mapping process, each word of a cache can store two or more words of main memory under the same index address. Each data word is stored along with its tag and the number of tag data pair in one word of cache is said to form a set. An example of set associative cache organization with set size of two is shown in figure.



The words stored at address 000000110010 and 010000110010 of main memory are stored in cache memory at index address 0000110010. Similarly, the words stored at address 010000111011 and 100000111011 of main memory are stored in cache memory at index address 0000111011. When CPU generates a memory request, the word is searched into cache with the help of index addresses.

Name of Setter: - Designation:-

Address:- Signature of Setter

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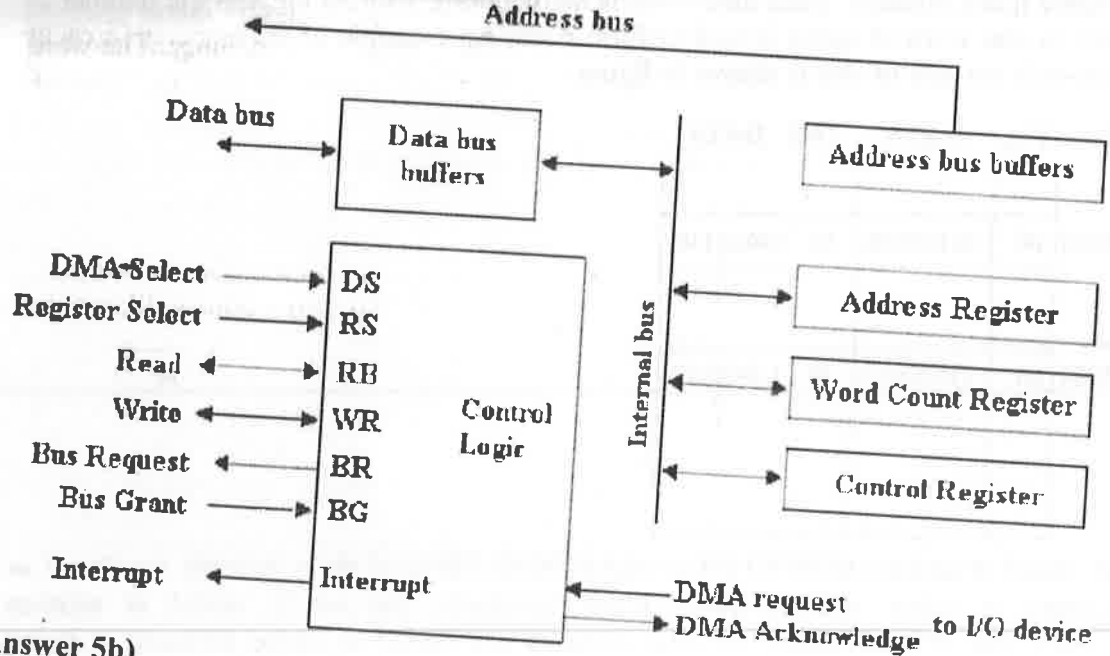
Sets (I) / (II)

Answer 5a)

The DMA controller consists of circuits of an interface to communicate with the CPU and I/O device. It also has an address register, a word count register, a set of address lines. The address register and address lines are used for direct communication with the memory. The word count register specifies the number of words that must be transferred. The figure shows the block diagram of DMA controller. The unit communicates with the CPU via the data bus and control lines. The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and RS (register select) inputs. When the BG (bus grant) input is 0, the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA registers. When BG=1, the CPU relinquished the buses and the DMA can communicate directly with the memory by specifying an address in the address bus and activating the RD or WR control.

The DMA controller has three registers. The address register contains an address to specify the desired location in memory and the address bits goes into the address bus through address bus buffers. The address register is incremented after each word that is transferred from/to memory. The word count register holds the number of words to be transferred to memory. This register is decremented by one after each word transferred from/to memory and internally tested for zero. The control register specifies the mode of transfer. All registers in DMA appears to the CPU as I/O interface registers and hence the CPU can read from or write into the DMA registers.



Answer 5b)

Segment	1	2	3	4	5	6	7	8	9	10	11	12	13

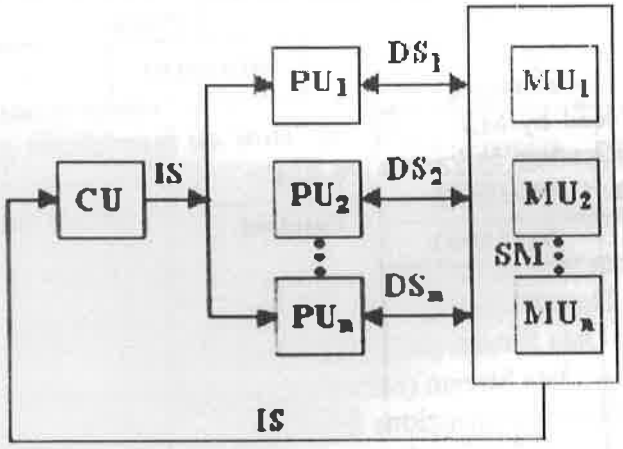
Name of Setter: -

Designation:-

Address:-

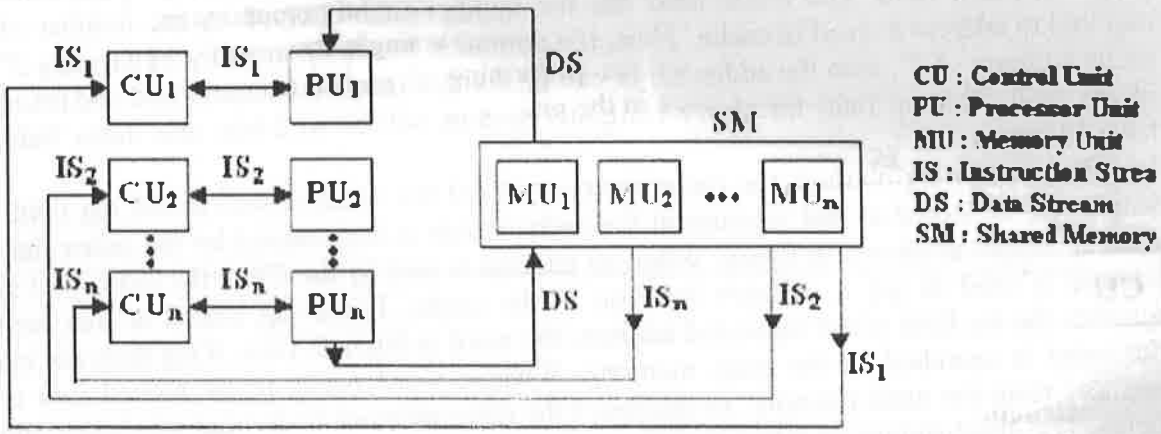
Signature of Setter

Examples are added a set of matrices simultaneously. Such computers are known as array processors. SIMD computer organization is shown in figure below.



Multiple Instruction Stream, Single Data Stream (MISD)

It refers to the computer in which several instructions manipulate the same data stream concurrently. In the structure different processing element run different programs on the same data. This type of processor may be generalized using a 2-dimensional arrangement of processing elements. Such a structure is known as systolic processor. MISD computer organization is shown in figure below.



Multiple Instruction Stream, Multiple Data Stream (MIMD)

MIMD computers are the general purpose parallel computers. Its organization refers to a computer system capable of processing several programs at a same time. MIMD systems include all multiprocessing systems. MIMD computer organization is shown in figure below.

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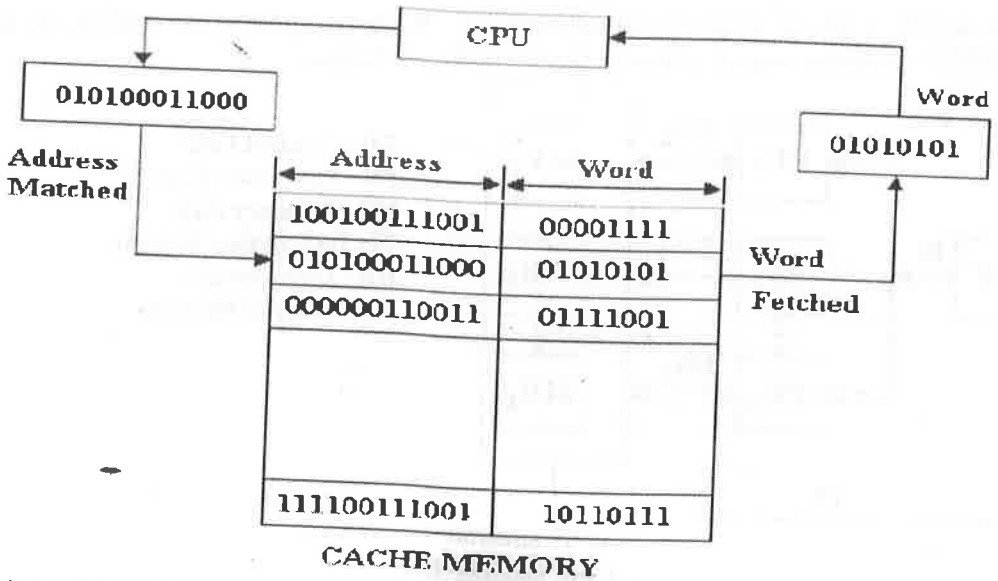
Model Answer

Subject:- Paper Code:-

Sets (I) / (II)



Direct Mapping

Suppose a computer has 4K main memory i.e. 4x1024 bytes and 1K cache memory. To address a word in the main memory, a 12 bit ($4K = 2^{12}$) address is required. Similarly, to address a word in the cache memory a 10-bit ($1K = 2^{10}$) address is required. Thus, a cache memory needs 10 bits to address a word and main memory requires 12 bits to address a word. In direct mapping method, the 12 bit address sent by CPU is divided into two parts called tag field and index field. The index field has the number of bits equal to the number of bits required to address a word in cache. Thus, if a computer has main memory of capacity 2^m and cache memory of 2^n, then the address bits will be divided into n bits index field and (m-n) bits of tag field. The tag field for above computer system will be of 2-bits and index field will have 10 bits.

In a direct mapping method, the cache memory stored the word as well as the tag field. The words will be stored at that location in the cache which is represented by the index fields of their addresses as shown in figure. When an address is sent by the CPU, the index part of the address is used to get a memory location in the cache. If the tag stored at that location matches the tag field of the requested address, the word is fetched. Else, if tag does not match, the word is searched in the main memory. When a word needs to be moved into cache memory from the main memory, its address I the main memory is divided into index and tag fields. The disadvantage of direct mapping is that the hit ratio can drop considerably if two or more words whose addresses have same index but different tags are accessed repeatedly.

Name of Setter: - Designation:-

Address:- Signature of Setter

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Model Answer

Paper Code:-

Subject:-

Sets (I) / (II)

Store T	M[T] ← AC
Load G	AC ← M[G]
Add H	AC ← AC + M[H]
Store Y	M[Y] ← AC
Load T	AC ← M[T]
Div Y	AC ← AC/M[Y]
Store Y	M[Y] ← AC

[illegible]

[illegible]

[illegible] A	TOS ← A
[illegible] B	TOS ← B
Sub	TOS ← A – B
[illegible] C	TOS ← C
Add	TOS ← A – B + C
Push G	TOS ← G
Push H	TOS ← H
Add	AC ← G + H
Div	TOS ← (A – B + C) / (G + H)
Pop Y	M[Y] ← TOS

Answer 8b)

Isolated I/O	Memory-Mapped I/O
i) I/O transfer is made through separate read and write line. ii) The I/O read and write control lines are enabled during the I/O are enabled during a memory transfer. iii) The isolated I/O configuration the CPU has distinct input and output instructions and each instruction is associated with the address of an interface register. iv) The isolated I/O method isolates memory and I/O address so that memory address values are not affected by interface address assignment.	i. Memory transfer is made through separate read and write lines. ii. The memory read and memory write control lines are enabled during a memory transfer. iii. Computer with memory mapped I/O can use memory type instructions to access I/O data. iv. In a memory mapped I/O organization theme are no specific input or output instructions.

Name of Setter: -

Designation:-

Address:-

Signature of Setter

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Sets (I) / (II)

Answer 7)

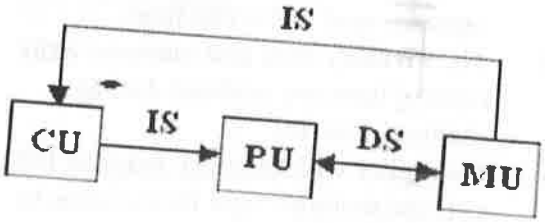
The classification based on the multiplicity of instruction streams and data streams in a computer system is known a Flynn's Classification. Parallel processing can be classified in variety of ways. It can be considered from the internal organization of the processors, from the interconnection structure between processors, or from the flow of information through the system. One classification was introduced by M.J. Flynn, as "How do instructions and data flow in the system?" and this classification is known as Flynn's Classification. Flynn's classified parallel computers into four categories based on how instructions process data. These categories are:

(i) Single Instruction Stream, Single Data Stream (SISD) Computer.
(ii) Single Instruction Stream, Multiple Data Stream (SIMD) Computer.
(iii) Multiple Instruction Stream, Single Data Stream (MISD) Computer.
(iv) Multiple Instruction Stream, Multiple Data Stream (MIMD) Computer.

The normal operation of a computer is to fetch instructions from memory and execute them in a processor. The sequence of instructions read from the memory constitutes an instruction stream. The operations performed on the data in the processor constitute a data stream. Parallel processing may occur in the instruction stream, in the data stream or in both.

Single Instruction Stream, Single Data Stream (SISD)

A computer with a single processor is called a Single Instruction Stream, Single Data Stream (SISD) Computer. It represents the organization of a single computer containing a control unit, a processor unit, and a memory unit. Instructions are executed sequentially and the system may or may not have internal parallel processing. Parallel processing may be achieved by means of a pipeline processing. In such a computer a single stream of instructions and a single stream of data are accessed by the processing elements from the main memory, processed and the results are stored back in the main memory. SISD computer organization is shown in figure below.



CU : Control Unit
PU : Processor Unit
MU : Memory Unit
IS : Instruction Stream
DS : Data Stream

Single Instruction Stream, Multiple Data Stream (SIMD)

It represents an organization of computer which has multiple processors under the supervision of a common control unit. All processors receive the same instruction from the control unit but operate on different items of the data. SIMD computers are used to solve many problems in science which require identical operations to be applied to different data set synchronously.

Name of Setter:-

Designation:-

Address:-

Signature of Setter

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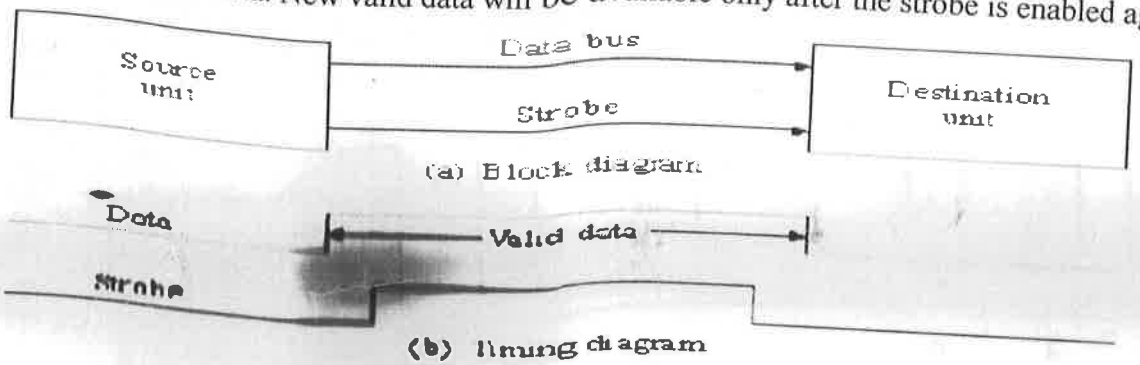
Sets (I) / (II)

Answer 9a)

The strobe control method of asynchronous data transfer employs a single control line to time each transfer. The strobe may be activated by either the source or the destination unit. The data bus carries the binary information from source unit to the destination unit. Typically, the bus has multiple lines to transfer an entire byte or word. The strobe is a single line that informs the destination unit when a valid data word is available in the bus.

In the timing diagram the source unit first places the data on the data bus. After a brief delay to ensure that the data settle to a steady value, the source activates the strobe pulse. The information on the data bus and the strobe signal remain in the active state for a sufficient time period to allow the destination unit to receive the data. The source removes the data from the bus a brief period after it disables its strobe pulse, which indicates that the data bus does not contain valid data. New valid data will be available only after the strobe is enabled again.



Source-initiated strobe for data transfer

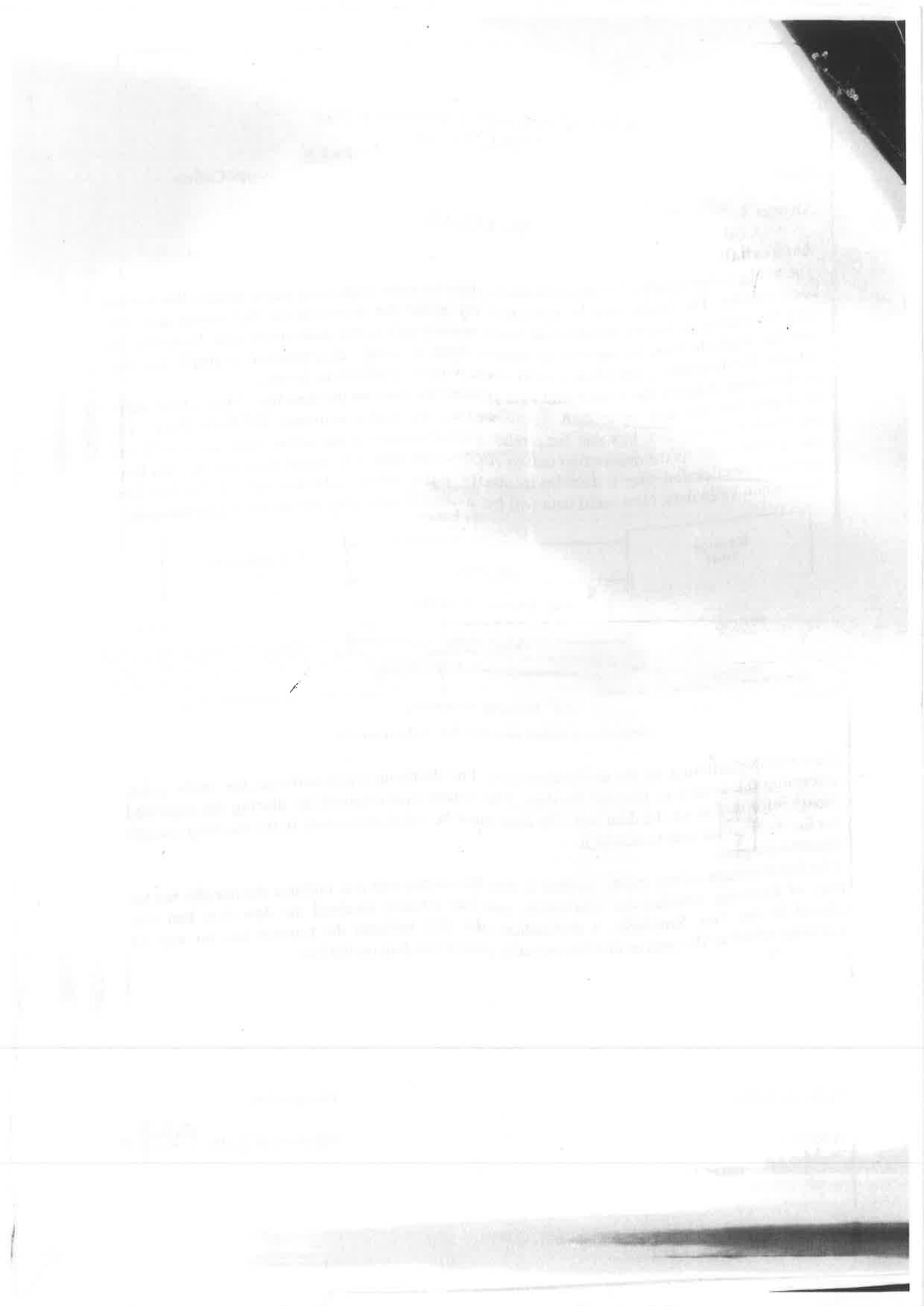
Data transfer initiated by the desintation unit. The destination unit activates the strobe pulse, informing the source to provide the data. The source unit responds by placing the requested binary information on the data bus. The data must be valid and remain in the bus long enough for the destination unit to accept it.

Disadvantages:-

The disadvantage of the strobe method is that the source unit that initiates the transfer has no way of knowing whether the destination unit has actually received the data item that was placed in the bus. Similarly, a destination unit that initiates the transfer has no way of knowing whether the source unit has actually placed the data on the bus.

Name of Setter: - Designation:-

Address:- Signature of Setter



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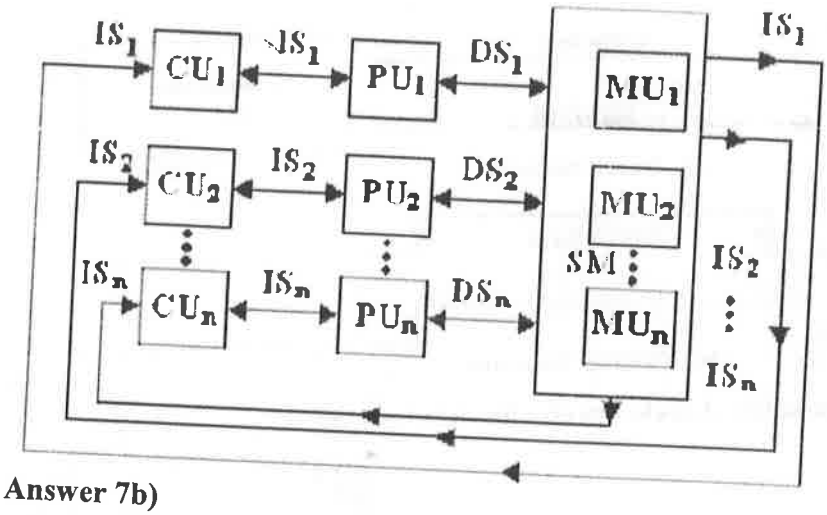
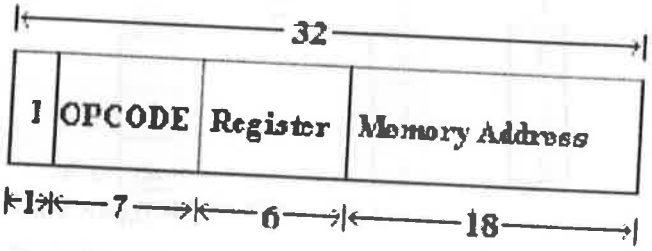
Sets (I) / (II)



Answer 7b)

(i)Memory unit = 256 K words = 2^{18} words
Hence, 18 bits is required to address one word of memory.
There are 64 registers i.e. 2^6 register
Hence, 6 bits are required to address one register.
1 bit is required for indirect bit.
Hence, 32 – (18+6+1) = 7 bits are required for operational code
(ii)



(iii) Data : 32 bits;
Address = 18 bits

Answer 8a)

(i) Using one address instruction

Load A AC ← M[A]
Sub B AC ← AC – M[B]
Add C AC ← AC + M[C]

Name of Setter: - Designation:-

Address:- Signature of Setter

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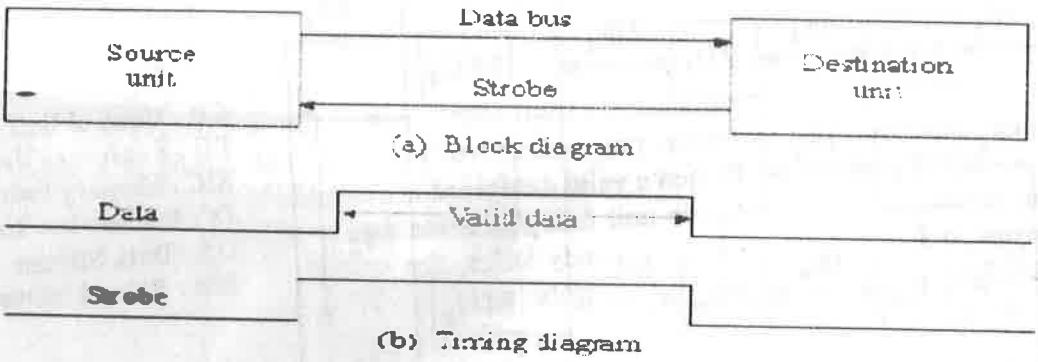
Model Answer

Subject:- **Paper Code:-**

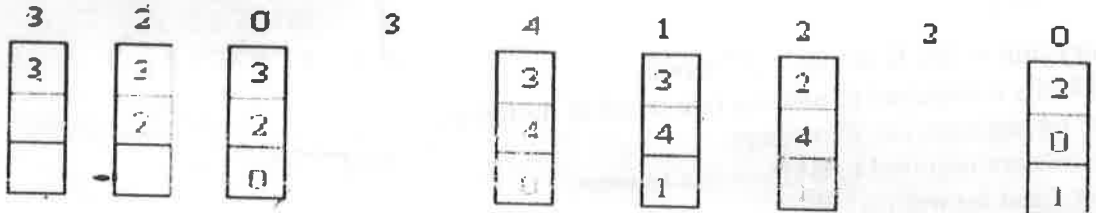
Sets (I) / (II)



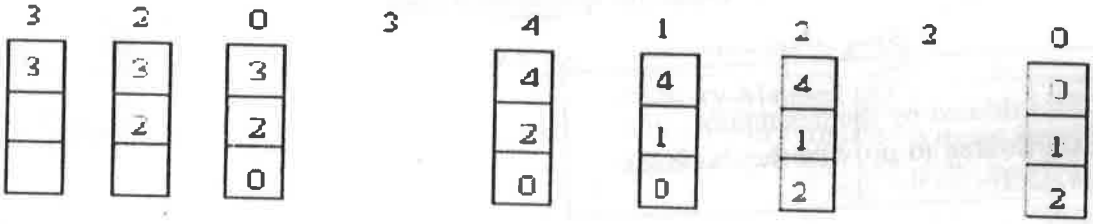
Destination-initiated strobe for data transfer

Answer 9b

(a) LRU



(b) FIFO



Name of Setter: -

Designation:-

Address:-

Signature of Setter